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(54) Title: **OVERLAY METROLOGY MARK**

(57) Abstract: An overlay metrology mark for determining the relative position between two or more layers of an integrated circuit structure comprising a first mark portion associated with and in particular developed on a first layer and a second mark portion associated with and in particular developed on a second layer, wherein the first and second mark portions together constitute, when the mark is properly aligned, at least one pair of test zones, each test zone comprising a first mark section formed as part of the first mark portion and a second mark section formed as part of the second mark portion each comprising a plurality of elongate rectangular mark structures in parallel array adjacently disposed to form the said test zone such that the mark structures in each test zone are in alignment in a first direction within the test zone but are substantially at 90° with respect to the mark structures of at least one other test zone in alignment in a second direction, and wherein the test zones making up the or each pair are laterally displaced relative to each other along one of the said directions. A method of marking and a method of determining overlay error are also described.



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